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This application is a continuation of and claims priority to U.S. Patent Application having an application number 10/122,524, filed 04/15/2002, which application is hereby incorporated by reference. (is now a U.S. Patent 6,717,442)

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention is related to the field of dynamic and static logic circuits, and more particularly to noise issues in dynamic to static conversion.

2. Description of the Related Art

Dynamic logic circuits are a circuit design tool often used in integrated circuits. Generally, dynamic logic circuits are precharged to a first state and then conditionally discharged to a second state according to one or more inputs. In contrast, static logic circuits continuously respond to inputs by driving the outputs to high or low states according to the state of the inputs. Since the inputs of dynamic logic circuits are only connected to the discharge transistors (as opposed to static logic circuitry in which a given input is typically connected to at least two transistors, one which may charge the output and one which may discharge the output), the capacitive load on the inputs may be comparatively lower than equivalent static logic circuitry. Additionally, the use of only discharge transistors may inherently speed the evaluation of the logic circuitry. Thus, dynamic logic circuitry may typically evaluate more rapidly than the corresponding static logic circuitry.

One complication introduced with the use of dynamic logic circuits is the need to convert the dynamic logic signals produced by the dynamic logic circuits to static logic signals when the dynamic logic signals are input to static circuitry, dynamic circuitry operating on a different phase of the clock, etc. In particular, the conversion hides the precharge of the dynamic circuitry during the precharge phase from the static circuitry,